Claims

[c1] A method of operating memory array with reduced noise coupling comprising:
providing a memory array having a plurality memory cells interconnected by wordlines, bitlines, and platelines, the memory cells of the array are arranged in a plurality of columns, a column comprises a bitline pair having first and second bitlines coupled to a sense amplifier;
performing a memory access to the array, the access selects one of the columns of memory cells; and
providing a plateline pulse to the selected column.

[c2] The method of claim 1 wherein the memory cells are ferroelectric memory cells.

[c3] The method of claim 2 wherein the memory cells of the array are arranged in an open bitline, a folded bitline, or a series architecture.

[c4] The method of claim 1 wherein the memory cells of the array are arranged in an open bitline, a folded bitline, or a series architecture.

[c5] The method claim 1 wherein unselected bitlines are set to a defined state.

[c6] The method of claim 5 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.

[c7] The method of claim 6 wherein the reference voltage is equal about $V_{DD}/2$.

[c8] The method of claim 7 wherein the non-selected bitlines are floated.

[c9] The method of claim 8 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c10] The method of claim 7 wherein the plateline pulse is equal to logic 1 or logic 0.

[c11] The method of claim 10 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c12] The method of claim 8 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c13] The method of claim 6 wherein the plateline pulse is equal to logic 1 or logic 0.

[c14] The method of claim 13 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c15] The method of claim 13 wherein the non-selected bitlines are floated.

[c16] The method of claim 15 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c17] The method of claim 5 wherein the plateline pulse is equal to logic 1 or logic 0.

[c18] The method of claim 17 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c19] The method of claim 17 wherein the non-selected bitlines are floated.

[c20] The method of claim 19 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c21] The method of claim 5 wherein the non-selected bitlines are floated.

[c22] The method of claim 6 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c23] The method of claim 5 wherein a plateline decoder coupled to the platelines provides the plateline pulse to the selected column.

[c24] The method of claim 1 wherein:
performing the memory access selects x columns of memory cells, where x is a whole number greater than 1, n adjacent columns of each selected column are unselected, where n is equal to at least 1; and
providing plateline pulses to the x selected columns.

[c25] The method of claim 24 wherein 1, some or all x columns are selected for outputting data during the memory access.

[c26] The method of claim 25 wherein the plateline pulses are equal to logic 1, logic 0, or a combination thereof.

[c27] The method claim 26 wherein unselected bitlines are set to a defined state.

[c28] The method of claim 27 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.

[c29] The method of claim 28 wherein the non-selected bitlines are floated.

[c30] The method of claim 27 wherein the non-selected bitlines are floated.

[c31] The method claim 25 wherein unselected bitlines are set to a defined state.

[c32] The method of claim 31 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.

[c33] The method of claim 32 wherein the non-selected bitlines are floated.

[c34] The method of claim 31 wherein the non-selected bitlines are floated.

[c35] The method of claim 24 wherein the plateline pulses are equal to logic 1, logic 0, or a combination thereof.

[c36] The method claim 35 wherein unselected bitlines are set to a defined state.

[c37] he method of claim 36 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.

[c38] 3he method of claim 37 wherein the non-selected bitlines are floated.

[c39] 3he method of claim 36 wherein the non-selected bitlines are floated.

[c40] 4he method claim 24 wherein unselected bitlines are set to a defined state.

[c41] 4he method of claim 40 wherein the defined state is selected to equal to logic 1, logic 0, reference voltage, or a combination thereof.

[c42] 4he method of claim 41 wherein the non-selected bitlines are floated.

[c43] 4he method of claim 40 wherein the non-selected bitlines are floated.